Digital Hilbert Transformers For Fpga Based Phase Locked

Digital Hilbert Transformers For Fpga Based Phase Locked Digital Hilbert Transformers for FPGABased PhaseLocked Loops Unlocking HighPerformance Synchronization The demand for highperformance lowlatency phaselocked loops PLLs is rapidly increasing across various applications including 5G communication radar systems and highspeed data acquisition Traditional analog PLLs struggle to meet the stringent requirements of these modern systems leading to a growing interest in FPGAbased digital PLLs Central to achieving optimal performance in these digital PLLs is the efficient implementation of the Hilbert transformer a crucial component for generating quadrature signals needed for precise phase control This blog post delves into the intricacies of implementing digital Hilbert transformers on FPGAs for improved phaselocked loop performance addressing common challenges and offering practical solutions The Problem Limitations of Traditional Analog and Simple Digital Hilbert Transformers Traditional analog PLLs suffer from several limitations including sensitivity to noise temperature drift and limited bandwidth While digital PLLs offer significant advantages in terms of flexibility programmability and stability efficient implementation of the Hilbert transformer within the FPGA remains a significant hurdle Naive digital Hilbert transformer implementations such as those using simple FIR filters often suffer from High resource consumption Direct implementation of a large FIR filter requires significant FPGA logic elements and memory limiting the achievable clock speeds and scalability Long latency Highorder FIR filters introduce significant latency hindering realtime applications demanding low latency synchronization Quantization errors Finite precision arithmetic within the FPGA introduces quantization errors that degrade the accuracy of the Hilbert transform and affect overall PLL performance Limited bandwidth Simple filter designs may not offer the necessary bandwidth for high frequency applications The Solution Advanced Techniques for Efficient FPGABased Digital Hilbert Transformers Addressing these limitations necessitates employing advanced techniques for implementing 2 digital Hilbert transformers on FPGAs Here are some promising approaches gaining traction in current research Optimized FIR Filter Designs Instead of using a straightforward FIR filter researchers are exploring optimized filter architectures Techniques like polyphase filter banks and optimized coefficient selection significantly reduce resource usage while maintaining desired accuracy These methods leverage the inherent parallelism of FPGAs for efficient implementation IIR FilterBased Hilbert Transformers Infinite Impulse Response IIR filters offer a potential advantage in terms of reduced computational complexity compared to FIR filters especially for highorder implementations However careful design is crucial to avoid stability issues and ensure sufficient accuracy Recent research explores stable IIR filter designs suitable for FPGA implementation minimizing resource consumption and latency HardwareAccelerated CORDIC Algorithms The Coordinate Rotation Digital Computer CORDIC algorithm is a powerful iterative algorithm for computing trigonometric functions Its suitability for parallel implementation in FPGAs makes it an attractive alternative for generating quadrature signals Efficient CORDIC implementations can achieve low latency and high precision with relatively low resource usage LookUp Table LUTBased Implementations For certain applications with limited bandwidth requirements LUTbased approaches can provide a simple and efficient solution Pre calculated values of the Hilbert transform are stored in the FPGAs memory enabling rapid retrieval and significantly reducing computation time However this approach is limited by memory capacity and resolution HighLevel Synthesis HLS Tools Utilizing HLS tools like Vivado HLS allows designers to specify the Hilbert transformer algorithm in highlevel languages like CC automatically generating optimized RTL code for FPGA implementation This approach simplifies design and allows for rapid prototyping and exploration of different algorithms and architectures Industry Insights and Expert Opinions Experts in the field emphasize the importance of considering the specific application requirements when selecting a suitable Hilbert transformer implementation The tradeoff between resource consumption latency accuracy and bandwidth needs to be carefully evaluated Moreover advancements in FPGA technology such as the introduction of high capacity memory and increased logic density are continuously expanding the possibilities for implementing sophisticated digital signal processing algorithms including advanced Hilbert transformers 3 Recent publications in journals like the IEEE Transactions on Circuits and Systems and IEEE Transactions on Signal Processing detail various innovative architectures for FPGAbased Hilbert transformers showcasing the ongoing progress in this domain Industry giants such as Xilinx and Intel are also actively contributing to the development of tools and IPs that simplify the implementation of such algorithms Conclusion The effective implementation of a digital Hilbert transformer is paramount for achieving high performance FPGAbased phaselocked loops While challenges exist regarding resource usage latency and quantization errors advanced techniques like optimized FIR filters IIR filters CORDIC algorithms LUTbased approaches and HLS tools offer powerful solutions By carefully considering applicationspecific constraints and leveraging the latest advancements in FPGA technology designers can successfully integrate highperformance digital Hilbert transformers into their PLL designs unlocking enhanced synchronization capabilities for demanding applications Frequently Asked Questions FAQs 1 What is the best algorithm for implementing a Hilbert transformer on an FPGA Theres no single best algorithm The optimal choice depends on the specific application requirements including bandwidth latency resource constraints and desired accuracy Consider the trade offs between FIR IIR CORDIC and LUTbased methods 2 How can I minimize quantization errors in my FPGAbased Hilbert transformer Employing higher precision arithmetic eg fixedpoint with increased bitwidth can reduce quantization errors Moreover careful scaling and normalization of signals within the algorithm can mitigate their effects 3 What are the typical resource requirements for an FPGAbased Hilbert transformer Resource usage varies greatly depending on the chosen algorithm and its implementation Highorder FIR filters consume significantly more resources than CORDICbased approaches Detailed estimations require specific algorithm and FPGA parameters 4 How can I ensure the stability of an IIRbased Hilbert transformer Proper design and analysis of the IIR filters poles are crucial for stability Employing established design techniques and tools for IIR filter design and verifying stability through simulations is essential 5 Are there any readily available IP cores for FPGAbased Hilbert transformers While several commercial and opensource IP cores exist their suitability depends on your specific needs 4 Its crucial to carefully evaluate the offered features and performance metrics to determine their appropriateness for your application However building a custom solution using HLS tools often offers greater flexibility and optimization

Logic Synthesis for FPGA-Based Mealy Finite State MachinesLogic Synthesis for FPGA-Based Finite State MachinesFPGA Based Accelerators for Financial ApplicationsApproximate Arithmetic Circuit Architectures for FPGA-based SystemsDesign of FPGA-Based Computing Systems with OpenCLBORPH: an Operating System for FPGA-based Reconfigurable ComputersFPGA-BASED Hardware AcceleratorsFPGA-based Implementation of Signal Processing SystemsReconfigurable ComputingLogic Synthesis for FPGA-Based Mealy Finite State MachinesFPGA-based System DesignHigh-Performance Computing Using FPGAsFPGA-based Implementation of Signal Processing SystemsFPGA-Based System DesignLogic Synthesis for FPGA-Based Control UnitsFPGA Based Design and ApplicationsFPGA-based Prototyping Methodology ManualArchitecture Exploration of FPGA Based Accelerators for BioInformatics ApplicationsIEEE Symposium on FPGAs for Custom Computing MachinesHigh-performance Coarse Operators for FPGA-based Computing Alexander Barkalov Alexander Barkalov Christian De Schryver Salim Ullah Hasitha Muthumala Waidyasooriya Hayden Kwok-Hay So Iouliia Skliarova Roger Woods Scott Hauck Alexander Barkalov Wayne Wolf Wim Vanderbauwhede Roger Woods Wayne Wolf Alexander Barkalov Arifur Rahman Doug Amos B. Sharat Chandra Varma Peter Athanas Matei Valentin Istoan

Logic Synthesis for FPGA-Based Mealy Finite State Machines Logic Synthesis for FPGA-Based Finite State Machines FPGA Based Accelerators for Financial Applications Approximate Arithmetic Circuit Architectures for FPGA-based Systems Design of FPGA-Based Computing Systems with OpenCL BORPH: an Operating System for FPGA-based Reconfigurable Computers FPGA-BASED Hardware Accelerators FPGA-based Implementation of Signal Processing Systems Reconfigurable Computing Logic Synthesis for FPGA-Based Mealy Finite State Machines FPGA-based System Design High-Performance Computing Using FPGAs FPGA-based Implementation of Signal Processing Systems FPGA-Based System Design Logic Synthesis for FPGA-Based Control Units FPGA Based Design and Applications FPGA-based Prototyping Methodology Manual Architecture Exploration of FPGA Based Accelerators for BioInformatics Applications IEEE Symposium on FPGAs for Custom Computing Machines High-performance Coarse Operators for FPGA-based Computing Alexander Barkalov Alexander Barkalov Christian De Schryver Salim Ullah Hasitha Muthumala Waidyasooriya Hayden Kwok-Hay So Iouliia Skliarova Roger Woods Scott Hauck Alexander Barkalov Wayne Wolf Wim Vanderbauwhede Roger Woods Wayne Wolf Alexander Barkalov Arifur Rahman Doug Amos B. Sharat Chandra Varma Peter Athanas Matei Valentin Istoan

this book is devoted to the logic synthesis of field programmable gate array fpga based circuits of mealy finite state machines fsm three new methods of state assignment are proposed which allows obtaining fsm circuits required minimum amount of internal chip resources logic synthesis for fpga based mealy finite state machines structural decomposition in logic design contains several original synthesis and optimization methods based on the structural decomposition of fpga based fsm circuits developed by the authors to optimize fsm circuits the authors introduce the use of three methods of state assignment twofold extended and composite these methods allow for the creation of two or three level architectures of fsm circuits the authors also demonstrate how the proposed methods fsm architectures and synthesis methods can replace known solutions based on either functional decomposition or classical methods of structural decomposition the authors also show how these architectures have regular systems of interconnections and demonstrate positive features compared to methods based on functional decomposition including producing circuits with fewer elements that are faster and consume less power than their counterparts the book includes experimental results proving the efficiency of the proposed solutions and compares the numbers in look up tables luts showing the performance maximum operating frequency and power consumption for various methods of state assignment the audience for this book is students researchers and engineers specializing in computer science engineering electronics and telecommunications it will be especially useful for engineers working within the scope of algorithms hardware based software accelerators and control units and systems based on the use of fpgas

this book discusses control units represented by the model of a finite state machine fsm it contains various original methods and takes into account the peculiarities of field programmable gate arrays fpga chips and a fsm model it shows that one of the peculiarities of fpga chips is the existence of embedded memory blocks emb the book is devoted to the solution of problems of logic synthesis and reduction of hardware amount in control units the book will be interesting and useful for researchers and phd students in the area of electrical engineering and computer science as well as for designers of modern digital systems

this book covers the latest approaches and results from reconfigurable computing architectures employed in the finance domain so called field programmable gate arrays fpgas have already shown to outperform standard cpu and gpu based computing architectures by far saving up to 99 of energy depending on the compute tasks renowned authors from financial mathematics computer architecture and finance business introduce the readers into today s challenges in finance it illustrate the most advanced approaches and use cases and present currently known methodologies for integrating fpgas in finance systems together with latest results the complete algorithm to hardware flow is covered holistically so this book serves as a hands on guide for it managers researchers and quants programmers who think about integrating fpgas into their current it systems

this book presents various novel architectures for fpga optimized accurate and approximate operators their detailed accuracy and performance analysis various techniques to model the behavior of approximate operators and thorough application level analysis to evaluate the impact of approximations on the final output quality and performance metrics as multiplication is one of the most commonly used and computationally expensive operations in various error resilient applications such as digital signal and image processing and machine learning algorithms this book particularly focuses on this operation the book starts by elaborating on the various sources of error resilience and opportunities available for approximations on various layers of the computation stack it then provides a detailed description of the state of the art approximate computing related works and highlights their limitations

this book provides wide knowledge about designing fpga based heterogeneous computing systems using a high level design environment based on opencl open computing language which is called opencl for fpga the opencl based design methodology will be the key technology to exploit the potential of fpgas in various applications such as low power embedded applications and high performance computing by understanding the opencl based design methodology readers can design an entire fpga based computing system more easily compared to the conventional hdl based design because opencl for fpga takes care of computation on a host data transfer between a host and an fpga computation on an fpga with a capable of accessing external ddr memories in the step by step way readers can understand followings how to set up the design environment how to write better codes systematically considering architectural constraints how to design practical applications

this book suggests and describes a number of fast parallel circuits for data vector processing using fpga based hardware accelerators three primary areas are covered searching sorting and counting in combinational and iterative networks these include the application of traditional structures that rely on comparators swappers as well as alternative networks with a variety of core elements such as adders logical gates and look up tables the iterative technique discussed in the book enables the sequential reuse of relatively large combinational blocks that execute many parallel operations with small propagation delays for each type of network discussed the main focus is on the step by step development of the architectures proposed from initial concepts to synthesizable hardware description language specifications each type of network is taken through several stages including modeling the desired functionality in software the retrieval and automatic conversion of key functions leading to specifications for optimized hardware modules the resulting specifications are then synthesized implemented and tested in fpgas using commercial design environments and prototyping boards the methods proposed can be used in a range of data processing applications including traditional sorting the extraction of maximum and minimum subsets from large data sets communication time data processing finding frequently occurring items in a set and hamming weight distance counters comparators the book is intended to be a valuable support material for university and industrial engineering courses that involve fpga based circuit and system design

the automation of the techniques for component architectural synthesis computational models and the reduction of energy consumption to help improve fpga performance are given in detail fpga based implementation of signal processing systems is an important reference for practising engineers and researchers working on the design and development of dsp systems for radio telecommunication information audio visual and security applications senior level electrical and computer engineering graduates taking courses in signal processing or digital signal processing shall also find this volume of interest book jacket

reconfigurable computing marks a revolutionary and hot topic that bridges the gap between the separate worlds of hardware and software design the key feature of reconfigurable computing is its groundbreaking ability to perform computations in hardware to increase performance while retaining the flexibility of a software solution reconfigurable computers serve as affordable fast and accurate tools for developing designs ranging from single chip architectures to multi chip and embedded systems scott hauck and andre dehon have assembled a group of the key experts in the fields of both hardware and software computing to provide an introduction to the entire range of issues relating to reconfigurable computing fpgas field programmable gate arrays act as the computing vehicles to implement this powerful technology readers will be guided into adopting a completely new way of handling existing design concerns and be able to make use of the vast opportunities possible with reconfigurable logic in this rapidly evolving field designed for both hardware and software programmers views of reconfigurable programming beyond standard programming languages broad set of case studies demonstrating how to use fpgas in novel and efficient ways

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learn the whys and hows of digital system design with fpgas from this thorough treatment up to date information and comparison of different modern fpga devices ieee fellow wayne wolf brings all related aspects of vlsi to fpga system design in this thorough introduction

high performance computing using fpga covers the area of high performance reconfigurable computing hprc this book provides an overview of architectures tools and applications for high performance reconfigurable computing hprc fpgas offer very high i o bandwidth and fine grained custom and flexible parallelism and with the ever increasing computational needs coupled with the frequency power wall the increasing maturity and capabilities of fpgas and the advent of multicore processors which has caused the acceptance of parallel computational models the part on architectures will introduce different fpga based hpc platforms attached co processor hprc architectures such as the chrec s novo g and epcc s maxwell systems tightly coupled hrpc architectures e g the convey hybrid core computer reconfigurably networked hprc architectures e g the qpace system and standalone hprc architectures such as epfl s confetti system the part on tools will focus on high level programming approaches for hprc with chapters on c to gate tools such as impulse c autoesl handel c mora c graphical tools matlab simulink ni labview domain specific languages languages for heterogeneous computing for example opencl microsoft s kiwi and alchemy projects the part on applications will present case from several application domains where hprc has been used successfully such as bioinformatics and computational biology financial computing stencil computations information retrieval lattice qcd astrophysics simulations weather and climate modeling

field programmable gate arrays fpgas are an increasingly popular technology for implementing digital signal processing dsp systems by allowing designers to create circuit architectures developed for the specific applications high levels of performance can be achieved for many dsp applications providing considerable improvements over conventional microprocessor and dedicated dsp processor solutions the book addresses the key issue in this process specifically the methods and tools needed for the design optimization and implementation of dsp systems in programmable fpga hardware it presents a review of the leading edge techniques in this field analyzing advanced dsp based design flows for both signal flow graph sfg based and dataflow based implementation system on chip soc aspects and future trends and challenges for fpgas the automation of the techniques for component architectural synthesis computational models and the reduction of energy consumption to help improve fpga performance are given in detail written from a system level design perspective and with a dsp focus the authors present many practical application examples of complex dsp implementation involving high performance computing e g matrix operations such as matrix multiplication high speed filtering including finite impulse response fir filters and wave digital filters wdfs adaptive filtering e g recursive least squares rls filtering transforms such as the fast fourier transform fft fpga based implementation of signal processing systems is an important reference for practising engineers and researchers working on the design and development of dsp systems for radio telecommunication information audio visual and security applications senior level electrical and computer engineering graduates taking courses in signal processing or digital signal processing shall also find this volume of interest everything fpga designers need to know about fpgas and vlsi digital designs once built in custom silicon are increasingly implemented in field programmable gate arrays fpgas effective fpga system design requires a strong understanding of vlsi issues and constraints and an understanding of the latest fpga specific techniques in this book princeton university s wayne wolf covers everything fpga designers need to know about all these topics both the how and the why wolf begins by introducing the essentials of vlsi fabrication circuits interconnects combinational and sequential logic design system architectures and more next he demonstrates how to reflect this vlsi knowledge in a state of the art design methodology that leverages fpga s most valuable characteristics while mitigating its limitations coverage includes how vlsi characteristics affect fpgas and fpga based logic design how classical logic design techniques relate to fpga based logic design understanding fpga fabrics the basic programmable structures of fpgas specifying and optimizing logic to address size speed and power consumption verilog vhdl and software tools for optimizing logic and designs the structure of large digital systems including register transfer design methodology building large scale platform and multi fpga systems a start to finish dsp case study addressing a wide range of design problems prentice hall professional technical reference upper saddle river nj 07458 phptr com isbn 0 13 142461 0

this book focuses on control units which are a vital part of modern digital systems and responsible for the efficiency of controlled systems the model of a finite state machine fsm is often used to represent the behavior of a control unit as a rule control units have irregular structures that make it impossible to design their logic circuits using the standard library cells design methods depend strongly on such factors as the fsm used specific features of the logic elements implemented in the fsm logic circuit and the characteristics of the control algorithm to be interpreted this book discusses moore and mealy fsms implemented with fpga chips including look up table elements lut and embedded memory blocks emb it is crucial to minimize the number of luts and embs in an fsm logic circuit as well as to make the interconnections between the logic elements more regular and various methods of structural decompositions can be used to solve this problem these methods are reduced to the presentation of an fsm circuit as a composition of different logic blocks the majority of which implement systems of intermediate logic functions different and much simpler than input memory functions and fsm output functions the structural decomposition results in multilevel fsm circuits having fewer logic elements than equivalent single level circuits the book describes well known methods of structural decomposition and proposes new ones examining their impact on the final amount of hardware in an fsm circuit it is of interest to students and postgraduates in the area of computer science as well as experts involved in designing digital systems with complex control units the proposed models and design methods open new possibilities for creating logic circuits of control units with an optimal amount of hardware and regular interconnections

this book covers advances in field programmable gate array fpga technologies focusing primarily on applications design methodology and technology evolution leading researchers and experts offer insights into state of the art fpgas and technology trends this book collects the best practices fpga based prototyping of soc and asic devices into one place for the first time drawing upon not only the authors own knowledge but also from leading practitioners worldwide in order to present a snapshot of best practices today and possibilities for the future the book is organized into chapters which appear in the same order as the tasks and decisions which are performed during an fpga based prototyping project we start by analyzing the challenges and benefits of fpga based prototyping and how they compare to other prototyping methods we present the current state of the available fpga technology and tools and how to get started on a project the fpmm also compares between home made and outsourced fpga platforms and how to analyze which will best meet the needs of a given project the central chapters deal with implementing an soc design in fpga technology including clocking conversion of memory partitioning multiplexing and handling ip amongst many other subjects the important subject of bringing up the design on the fpga boards is covered next including the introduction of the real design into the board running embedded software upon it in and debugging and iterating in a lab environment finally we explore how the fpga based prototype can be linked into other verification methodologies including rtl simulation and virtual models in systemc along the way the reader will discover that an adoption of fpga based prototyping from the beginning of a project and an approach we call design for prototyping will greatly increase the success of the prototype and the whole soc project especially the embedded software portion design for prototyping is introduced and explained and promoted as a manifesto for better soc design readers can approach the subjects from a number of directions some will be experienced with many of the tasks involved in fpga based prototyping but are looking for new insights and ideas others will be relatively new to the subject but experienced in other verification methodologies still others may be project leaders who need to understand if and how the benefits of fpga based prototyping apply to their next soc project we have tried to make each subject chapter relatively standalone or where necessary make numerous forward and backward references between subjects and provide recaps of certain key subjects we hope you like the book and we look forward to seeing you on the fpmm on line community soon go to synopsys com fpmm

this book presents an evaluation methodology to design future fpga fabrics incorporating hard embedded blocks hebs to accelerate applications this methodology will be useful for selection of blocks to be embedded into the fabric and for evaluating the performance gain that can be achieved by such an embedding the authors illustrate the use of their methodology by studying the impact of hebs on two important bioinformatics applications protein docking and genome assembly the book also explains how the respective hebs are designed and how hardware implementation of the application is done using these hebs it shows that significant speedups can be achieved over pure software implementations by using such fpga based accelerators the methodology presented in this book may also be used for designing hebs for accelerating software implementations in other domains besides bioinformatics this book will prove useful to students researchers and practicing engineers alike

field programmable gate arrays fpgas have been shown to sometimes outperform mainstream microprocessors the circuit paradigm enables efficient application specific parallel computations fpgas also enable arithmetic efficiency a bit is only computed if it is useful to the final result to achieve this fpga arithmetic shouldn t be limited to basic arithmetic operations offered by microprocessors this thesis studies the implementation of coarser operations on fpgas in three main directions new fpga specific approaches for evaluating the sine cosine and the arctangent have been developed each function is tuned for its context and is as versatile and flexible as possible arithmetic efficiency requires error analysis and parameter tuning and a fine understanding of the algorithms used digital filters are an important family of coarse operators resembling elementary functions they can be specified at a high level as a transfer function with constraints on the signal noise ratio and then be implemented as an arithmetic datapath based on additions and multiplications the main result is a method which transforms a high level specification into a filter in an automated way the first step is building an efficient method for computing sums of products by constants based on this fir and iir filter generators are constructed for arithmetic operators to achieve maximum performance context specific pipelining is required even if the designer s knowledge is of great help when building and pipelining an arithmetic datapath this remains complex and error prone a user directed automated method for pipelining has been developed this thesis provides a generator of high quality ready made operators for coarse computing cores which brings fpga based computing a step closer to mainstream adoption the cores are part of an open ended generator where functions are described as high level objects such as mathematical expressions

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